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REAL TIME ECG MONITORING SYSTEM: A NOVEL ARCHITECTURE OF SQUARING CIRCUIT FOR SPECTRAL ESTIMATION

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ABSTRACT: *In the current fast moving world, all are seeking for a faster device with accuracy. This paper proposed a real-time ECG monitoring system, which is faster compared to other existing ECG monitoring system. Existing module uses normal squaring circuits using array multiplier, booth multiplier or modified booth multiplier. But in this paper, we have used the vedic multiplier and squarer to improve the efficiency of the system. It is difficult to implement a polynomial filer but quadratic filter is easy to implement than polynomial filter. Because quadratic filter will produce the result in a compact form were polynomial is used for deriving a spectrum. When a sinusoidal signal passes through the channel, the quadratic and cubic term gives rise to non-linear distortion such as harmonic and inter-modulation distortion. Xilinx software is used to implement and obtain digitize signals in signal power. This project is to implement a squaring operation which is involved in a quadratic filter using FPGA. Because the field programmable gate array is most suitable for real time application and spectral estimation. Implementation of FIR filters in poly-phase structure since the structure is efficient and easy to implement. FIR filter is used to detect the distortion in the system. Real time quadratic filter is used for spectral estimation.*

Keywords-Vedic Multiplier, Vedic Squarer, FFT, FIR

I INTRODUCTION

Polynomial filters are required for non-linear system at which the performances of linear filters are failed miserably is that of trying to relate two signals with non-overlapping spectral component. In non-linear filters the accuracy will be less. It can be improved by volterra series. Volterra kernel depends on the order of truncated volterra series. Adaptive Algorithm is widely used for the kernel estimation. Volterra series are similar to Taylor series with memory. It is difficult to implement a polynomial filer but quadratic filter is easy to implement than polynomial filter. Because quadratic filter will produce the result in a compact form were polynomial is used for deriving a spectrum. When a sinusoidal signal passes through the channel, the quadratic and cubic term gives rise to non-linear distortion such as harmonic and inter-modulation distortion. The design of 8-bit squaring circuit is programmed and implemented using Verilog in Xilinx. Here in 8-bit squaring circuit Vedic multiplier is used in order to reduce the number of delays in the 8-bit squaring circuit. So it produces an efficient result. The 8-bit squaring module output is applied to the FIR filter the FIR filter is designed using poly-phase structure, which removes noise, distortion and produces efficient result. The FIR output is applied to the FFT. FFT is used to combine the frequency spectra and time domain to display the frequency spectrum and it produce the output in fastest manner. The major function of proposed system is to square the given input signal and to display the spectrum. In real time system, this can be implemented effectively and used in medical field application like ECG, EEG, and Echo cancellation.

II OVERALL BLOCK DIAGRAM

The proposed system consists of following module are listed below:

- Squaring module
- FIR module
- FFT module

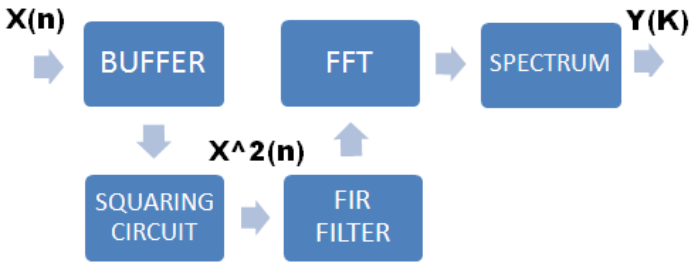

Fig. 1 Overall Block Diagram

An analog input signal (for example Heart Beats) is converted into digital using analog to digital converter. And the output signal of analog to digital converter is stored in the buffer. The signals from the

buffer are squared using 8-bit squaring circuit. The design of 8-bit squaring circuit is programmed and implemented using Verilog in Xilinx. The implementation of 8-bit squaring circuit in digital hardware in real time system is a difficult task. Here in 8-bit squaring circuit Vedic multiplier is used to reduce the number of delays produced in the 8-bit squaring circuit. So it produces an efficient result. The 8-bit squaring module output is applied to the FIR filter. The FIR filter is designed using poly-phase structure, which removes noise, distortion and produces efficient result. The FIR output is applied to the FFT. FFT is used to combine the frequency spectra and time domain to display the frequency spectrum and it produce the output in fastest manner.

III SQUARING MODULE

Multiplication and squaring are most common and important arithmetic operations having wide applications in different areas of engineering and technology. The performance of any circuit is evaluated mainly by estimating the silicon area and speed (delay). Hence, continuous efforts are being made to achieve the same. In order to calculate the square of a binary number, fast multipliers such as Braun Array, Baugh-Wooley methods of two's compliment, Booth's algorithm using recorded multiplier and Wallace trees are in use. Recursive decomposition and Booth's algorithm are the most successful algorithms used for multiplication. Other methods include Vedic multipliers based on 'UrdhvaTiryagbhyam' and the "Duplex" properties of 'UrdhvaTiryagbhyam'. Therefore, the main motivation behind this work is to investigate the VLSI Design and Implementation of Squaring Circuit architecture with reduced delay. Only one multiplier is used here instead of four multipliers and one squaring circuit is used twice to reduce delay.

2X2 MULTIPLIER

Here, an efficient Vedic multiplier using carry save adder is presented. The 2X2 Vedic multiplier module is implemented using two half-adder modules and is displayed in Fig. 2. Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated. It is wise to write Implementation Equations of 2X2 Vedic multiplier module for simulation.

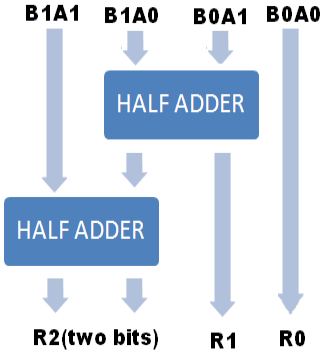

Fig.2 Architecture of 2x2 Vedic Multiplier

2-Bit Squaring Circuit

The 2X2 Vedic multiplier architecture is modified as to realize the 2-bit squaring circuit as shown in the fig.3. Here, one half adder and one AND gate are utilized instead of two half-adders. Thus, we have saved one XOR gate.

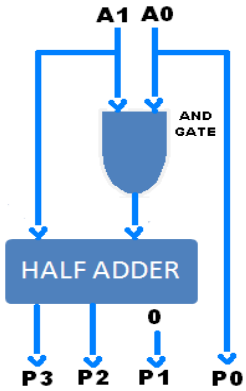

Fig.3 2-Bit Vedic Squaring Circuit

4X4 MULPLIER

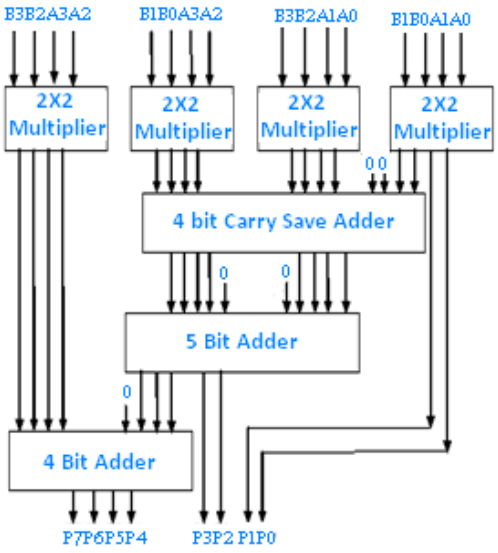

Fig.4 Architecture of 4X4 Vedic multiplier

The 4X4 Vedic multiplier architecture is displayed in Fig.4. This is implemented using four 2X2 Vedic multiplier modules as discussed. The

beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This, in turn, reduces delay. Here the architecture of 4X4 multiplier using Vedic method is described. To get final product (P7P6P5P4P3P2P1P0), one 4-bit carry save adder, one 5-bit binary adder and one 4-bit binary adder are used. In this proposal, the 4-bit carry save adder (CSA) is used to add three 4-bit operands. i.e. concatenated 4-bit ("00" & most significant two output bits of right hand most of 2X2 multiplier module as shown in Fig.2) and two 4-bit operands we get from the output of two middle multiplier modules. It may be noted that the outputs of the CSA (sum and carry) are fed into a 5-bit binary adder to generate 5-bit sum, as desired. Many more interesting ideas can be revoked here. It may be reiterated the fact that the middle part (P3P2) denotes the least significant two bits of 5-bit sum obtained from the 5-bit binary adder. Finally, as shown in Fig.4, the 4-bit output of the left most 2X2 multiplier module and concatenated 4-bits ('0' & the most significant three bits of 5-bit sum) are fed into a 4-bit binary adder. In this architecture, the P7P6P5P4 express the sum. The proposed Vedic multiplier can be used to reduce delay. Early literature speaks about Vedic multipliers based on array multiplier structures. On the other hand, we proposed a new architecture, which is efficient in terms of speed. The arrangements of CSA and binary adders shown help us to reduce dely. Interestingly, 8X8 Vedic multiplier modules is implemented easily by using four 4X4 multiplier modules. Further, the proposed 4X4 Vedic multiplier can also be used for squaring of a 4-bit binary number.

8-BIT SQUARING CIRCUITS

The 8-bit squaring circuit and 16-bit squaring circuits are implemented using Vedic multiplier module and squaring circuits of 4-bit and 8-bit, respectively. Likewise, n-bit squaring circuit can be implemented taking one (n/2)-bit Vedic multiplier module and two (n/2)-bit squaring circuits. The performance of the proposed squaring circuit using Vedic Mathematics proved to be efficient in terms of speed. Due to its regular and parallel structure, it can be realized easily on silicon as well. Squaring of binary numbers of bit size other than powers of 2 can also be realized easily. For example, squaring of a 24-bit binary number can be found by using 32- bit squaring circuit with 8 MSBs (of inputs) as zero. The idea proposed here may set path for future research in this direction. Future scope of research is to reduce area requirements.

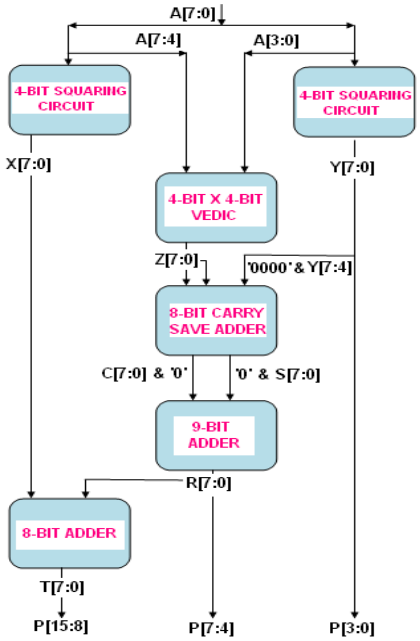

Fig.5 Architecture of 8-bit Vedic squaring circuit

IV FIR MODULE

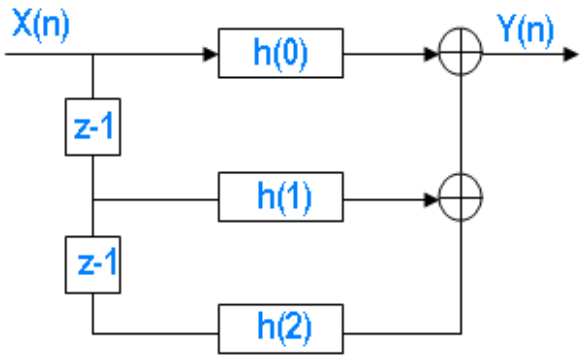

Fig.6 FIR filter using poly-phase structure

The finite impulse response (FIR) digital filter is a spatial domain filter with a frequency domain representation. The theory of the FIR filter is presented and techniques are described for designing FIR filters with known frequency response characteristics. Rational design principles are emphasized based on characterization of the imaging system using the modulation transfer function and physical properties of the imaged objects. Band pass, Wiener, and low-pass filters were designed and applied to T1 myocardial images. The band pass filter eliminates low-frequency image components that represent background activity and high-frequency components due to noise. The Wiener, or minimum mean square error filter 'sharpens' the image while also reducing noise. The Wiener filter illustrates the power of the FIR technique to design filters with any desired frequency response. The low pass filter, while of relative limited use, is presented to compare it with a popular elementary 'smoothing' filter. "Poly-phase Filters" is often incorrectly taken to mean some

special kind of filter instead; it is merely a special structure that is handy when using filters in multi-rate settings.

V FFT MODULE

Fast Fourier Transform (FFT) algorithms have computational complexity O(n log n) instead of $O(n^2)$. If n is a power of 2, a one-dimensional FFT of length n requires less than $3n \log_2 n$ floating-point operations (times a proportionality constant). For n = 220, that is a factor of almost 35,000 faster than $2n^2$.

The MATLAB® functions FFT, FFT2, and FFTn (and their inverses IFFT, IFFT2, and IFFTn, respectively) all use fast Fourier transform algorithms to compute the DFT.

When using FFT algorithms, a distinction is made between the window length and the transform length. The window length is the length of the input data vector. It is determined by, for example, the size of an external buffer. The transform length is the length of the output, the computed DFT. An FFT algorithm pads or chops the input to achieve the desired transform length. The fig.7 will illustrate the two lengths.

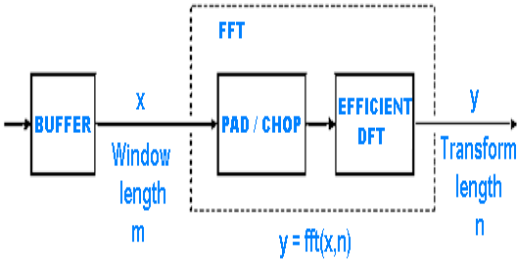

Fig.7 Block Diagram of FFT

The execution time of an FFT algorithm depends on the transform length. It is fastest when the transform length is a power of two, and almost as fast when the transform length has only small prime factors. It is typically slower for transform lengths that are prime or have large prime factors. Time differences, however, are reduced to insignificance by modern FFT algorithms such as those used in MATLAB

VI SIMULATION & RESULT

8-BIT SQUARING CIRCUIT

In 8-bit squaring circuit A is the input which is 8-bit and P is the output which is 16-bit.The implementation of 8-bit squaring circuit is simulated using Xilinx in VLSI. To implement the block diagram of 8-bit squaring circuit contain two 4bit squarer, one 4x4 multiplier, 8-bit carry save adder, one 8bit ripple carry adder and 9bitripple carry adder is used.

FINITE IMPULSE RESPONSE

The 8-bit squaring circuit which was implemented above is given as the input to FIR filter. The FIR filter is act as the low pass filter so which detects the high frequency signal component and gives the finite range of output as the result which was simulated.

FAST FOURIER TRANSFORM

In FFT the N number of sequence is given as the input and spectrum was the output .The FFT that combines the N number of time domain and the N number of frequency spectra and displays the result into frequency domain. The spectrum of FFT was implemented in MAT LAB

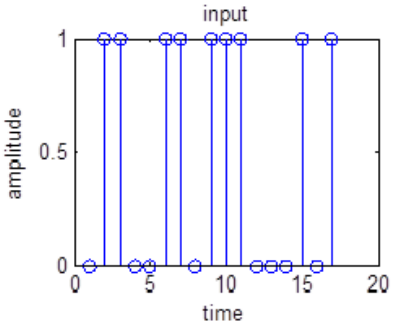

Fig.8 Signal Obtained from FIR

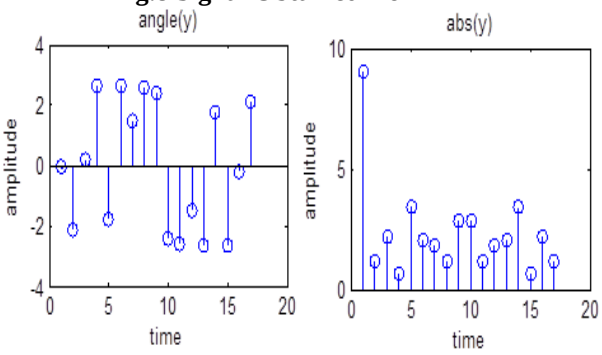

Fig.9 Magnitude and Phase values of the input toFFT

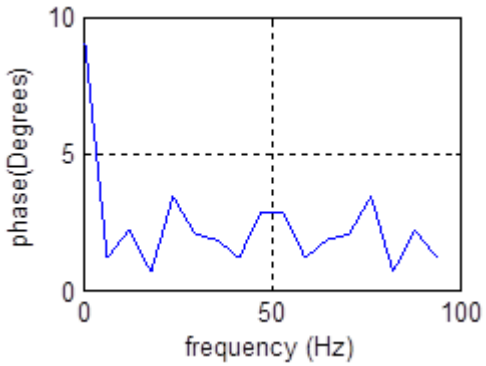

Fig.10 Spectrum of FFT

VII CONCLUSION

Thus this paper is more useful in medical field application to display the spectrum and to squaring the given input signal in most fast and more efficient manner and we can also hear the sound of the signals from the spectrum compared to other spectrum like ECG,EEG it is more effective because the spectrum of EEG,ECG can be connect to their

own device, but the spectrum which has been found in this paper can be connected to any device to display the needed spectrum none of the spectrum has been found to square the given signal without the cardiac process. But in this paper the squaring can be done and the spectrum was displayed without using the cardiac process. The cardiac process is more expensive so the cost the spectrum, which is found in this paper, was less. So one of the advantage is the middle level people can also buy this spectrum displayer and another advantage is that it is portable.

REFERENCES

[1] Kabirajsethi "An Improved Squaring Circuit for Binary Numbers",Department of Electronics and Teleconnunication engineering (IJACSA) International Journal of Advanced Computer Science and Applications, Vol. 3, No.2, 2012

[2] Datla. S.R"A Low Power High Performance Radix-4 Approximate Squaring Circuit", Application-specific Systems, Architectures and Processors 2009. ASAP 2009 20th IEEE International Conference.

[3] Deshpande. A,"Squaring units and a comarison with multipliers", Circuits and Systems (MWSCAS), 2010 53rd IEEE International Midwest Symposium

[4] Ryan j. tibshirani "Adaptive Piecewise Polynomial Estimation via Trend Filtering", [math.ST] 10 Apr 2013

[5] Poornima M, Shiva raj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H"Implementation of Multiplier using Vedic Algorithm", International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013

[6] Dr. raaedfalehhassan, alisubhiabbood"Design and Implementation of FPGA based Adaptive Filter", The International Journal of Engineering, June 2013.

[7] Jose m. gilcacho "Linear-in-the-parameters nonlinear adaptive filters for loudspeaker modeling in acoustic echo cancellation", J. Audio Eng. Sco., Vol. 1, No. 1, 2013 July 1

[8] Jalaja.s"High Speed VLSI Architecture for Squaring Algorithm Using Retiming Approach", Advances in Computing and Communications (ICACC), 2013 Third International Conference

[9] Kuan-Ju Huang "A pipeline VLSI design of fast singular value decomposition processor for real-time EEG system based on on-line recursive independent component analysis", Dept. of Electr. Eng., Nat. Chiao Tung University Hsinchu, Taiwan 2013

[10] Tsoumanis, K "An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator", School of Electrical and Computer Engineering, National Technical University of Athens (NTUA), Athens, Greece