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Reducing Area and Power Dissipation in NoC using Data Encoding Techniques

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Abstract—As technology shrivel, the power dissipated by the links of a network-on-chip (NoC) starts to compete with the power dissipated by the other elements, such as, the routers and the network interfaces (NIs).In this paper, we present a set of data encoding schemes aimed at reducing the Area and Power dissipation by the links of an NoC. The proposed schemes are designed by Encoder and Decoder block of the system. Then it will be reducing the area of the Encoder and Decoder blocks in NoC.

Index Terms— data encoding, Interconnection on chip, Network-on-chip (NoC), Modelsim, Verilog.

INTRODUCTON

Network on Chip are emerging for the developing the exceptionally dependable for correspondence framework stage. NoC enhances the adaptability of SoCs and the low force of complex SoCs contrasted with different plans.The wires in the connections of the NoC are imparted by numerous signs. As the quality of coordinated frameworks continue growing ,a NoC gives enhanced upgraded execution (such as throughput) and adaptability in correlation with past correspondence architectures (e.g., allocated point-to-point signal wires, shared buses or segmented buses with bridges).In existing strategy traditional switch is intended to its related systems through ports. The switch uses directing tables to track which system are joined with its ports. It gets a bundle, gets the packet's destination location, and afterward quests its directing table to figure out which of its ports is connected with that destination address. Steering tables thusly store the location and related port number of each system for which they course activity.

In this work, we are going to reducing the power dissipation in the network links. The power dissipation in the network on chip is relevant to the power dissipation in the routers and Network Interfaces(NIs). For highly integrated electronic systems, the reduction of on-chip power dissipation is a essential one. The amount of power consumption in a NOC grows linearly by increasing the amount of bit transitions in consequent data packets sent through the interconnect architecture. By using the coding schemes we are reducing the switching activity on both wires and logic in this way we are reducing the power consumption in the NOC. The power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity [2]. Data encoding is mainly used for reducing the number of bit transition over interconnects.

II.RELATED WORKS

In the next several years, the availability of the chips with 1000 cores is foreseen [6]. In these chips, a significant fraction of the total system power budget is dissipated by interconnection network. Therefore, the design of power efficient interconnection networks has been the focus of many works published in the literature dealing with NoC architecture. These works concentrate on different components of the interconnection networks such as routers, NI, and links. Since the focus of this paper is on reducing the power dissipation by the links, in this section, briefly review some of the works in the area of link power reduction. These include the techniques that make use of shielding [7], [8], increasing line-to-line spacing [9], [10], repeater insertion [11]. They all increases the chip area. The data encoding scheme is another method that was employed to reducing the link

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power dissipation. The data encoding techniques may be classified into two types. In the first type, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity. In this type, bus invert (BI) [12] and INC-XOR [13] have been proposed for the case that random data patterns are transmitted through these lines. On the other hand, gray code [14], T0[15], working-zone encoding [16], and T0-XOR [17] were suggested for the case of correlated data patterns. Application specific approaches have also been proposed [18]–[22].This category of encoding is not suitable to applied in the deep submicron meter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption, making the above mentioned techniques, which ignore such contributions, inefficient[23].The works in the second type concentrate on reducing power dissipation through the reduction of the coupling switching [10], [22] Among these schemes [10], [24]– [28], the switching activity is reduced using many extra control lines.For example, data bus width grows from 32 to 55 in [24]. The techniques proposed in [20] have a smaller number of control lines but the complexity of their decoding logic is high. The technique is described as follows: first, the data are both odd inverted and even inverted, and the transmission is performed using the kind of inversion that reduces more the switching activity.

Let us now discuss in more detail the works with which we compare our proposed data encoding schemes. In [12], the number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link.

This technique is only concerned about the self-switching without worrying the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably larger (e.g., four times) compared with the self-capacitance, and should be considered in any scheme proposed for the link power reduction.

TABLE I
EFFECT OF ODD INVERSION ON CHANGE OF TRANSITION TYPES

Time	Normal		Odd Inverted			
$t-1$	Type I		Types II, III, and IV			
t	00, 11 00, 11, 01, 10		01, 10 00, 11		00, 11, 01, 10	01, 10
	10, 01 01, 10, 00, 11		11, 00 11, 00		00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type I		Type I			
t	01, 10		01, 10			
	10, 01		11, 00			
$t-1$	Type III		Type I			
t	00, 11		00, 11			
	11, 00		10, 01			
$t-1$	Type IV		Type I			
t	00, 11, 01, 10		00, 11, 01, 10			
	00, 11, 01, 10		01, 10, 00, 11			

In this method, a complex encoder counts the number of Type I (Table I) transitions with a weighting coefficient of one and the number of Type II transitions with the weighting coefficient of two. If the number is larger than half of the link width, the inversion will be performed. In addition to the complex encoder, the technique only works on the patterns whose full inversion leads to the link power reduction while not considering the patterns whose full inversions may lead to higher link power consumption. Therefore, the link power reduction achieved through this technique is not as large as it could be. This scheme was also based on the hop-by-hop technique. In another coding technique presented in [25], bunches of four bits are encoded with five bits. The encoded bits were isolated using shielding wires such that the occurrence of the patterns "101" and "010" were prevented. This way, no simultaneous Type II transitions in two adjacent pair bits are induced. This technique effectively reduces the coupling switching activity. Although the technique reduces the power consumption considerably, it increases the data transfer time, and, hence, the link energy consumption. This is due to the fact that for each four bits, six bits are transmitted which increases the communication traffic. This technique was also based on the hop-by-hop approach. A coding technique that reduces the coupling switching activity by taking the advantage of end-to-end encoding for wormhole switching has been presented in [23]. It is based on lowering the coupling switching activity by eliminating only Type II transitions. In this paper, we present three encoding schemes. In Scheme I, we focus on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Finally, in Scheme III, we consider the fact that Type I transitions show different behaviors in the case of odd and even inverts and make the inversion which leads to the higher power saving.

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III PROPOSED ENCODING SCHEMES

In this section, present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activity on the links of the interconnection network. Let us first describe the power model that contains the different components of power dissipation of a link.. One can classify four types of coupling transitions. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high, other makes transition from high to low .A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type and hence, the coupling transition activity, is a weighted sum of different types of coupling transition contributions .Here, we calculate the occurrence probability for different types of transitions. Consider that flit (t − 1) and flit (t) refer to the previous flit which was transferred through the link and the flit is about to pass through the link, respectively.We consider only two adjacent bits of the physical channel.Sixteen different combinations of these four bits could occur (Table I). Note that the first bit is the value of the generic i th line of the link, whereas the second bit represents the value of its (i + 1)th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, we present three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

A SCHEME I:

In Scheme I, we focus on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Finally, in Scheme III, we consider the fact that Type I transitions show different behaviors in the case of odd and even invert and make the inversion which leads to the higher power saving.

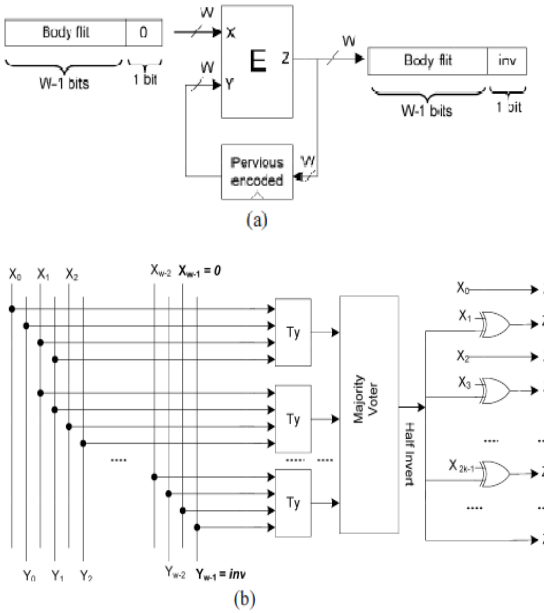

Fig.1. a) Block diagram of Encoder Scheme I
b) Internal view of Encoder Block Scheme I

The general block diagram in Fig. 1(a) is same for scheme 1, scheme 2 and scheme 3. The w-1 bit is given to the one input block. This block converts the original binary input into encoding output.The encoder block compares these two inputs and performing the any one of the inversion based on the transition types. The block E is vary for all the three schemes. Comparing the current data and previous encoded data to decide which inversion is performed for link power reduction. Here the TY block this takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs, whether more number of type 1 and type 2 transitions is occurring means it set the output state to 1, otherwise it set the output to 0. The odd inversion is performed for these type of transitions. The last stage using the XOR circuits, these circuit is used to perform the inversion on odd bits. The decoding is performed by simply inverts the encoder circuit when the inverting bit is high.

B SCHEME II:

In scheme II, our main goal is to reducing the number of Type II transitions. Type II transitions are converted into Type IV transitions. This scheme compares the two data‘s based on to reducing the link power reduction by doing full inversion or odd inversion or no inversion operation.

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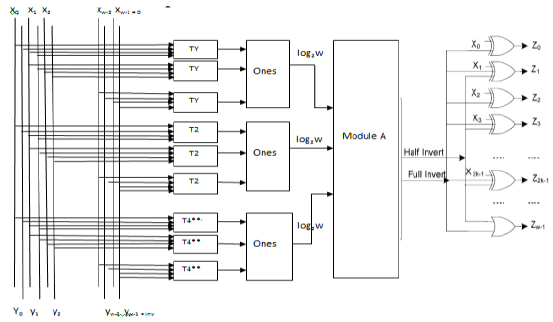

Fig.2. Encoder Architecture Scheme II

Full and odd inversion based this advanced encoding architecture consist of w-1 link width and one bit for inversion bit which indicate if the bit travel through the link is inverted or not. W bits link width is considered when there is no encoding is applied for the input bits. Here the TY block from scheme 1 is added in scheme 2. This takes two adjacent bits from the given inputs. From these two input bits the TY block checks what type of transitions occurs. We have T2 and T_{4}^{**} blocks which determines if any of the transition types T2 and T_{4}^{**}occur based on the link power reduction. The number of ones blocks in the next stage. The output of the TY, T2 and T_{4}^{**} send through the number of one's blocks. The output of the ones block is log 2 w. The first ones block is used to determine the number of transitions based on odd inversion. The second ones block determines the number of transitions based on the full inversion and the then another one ones block is used to determine the number of transitions based on the full inversion. These inversions are performed based on the link power reduction. Based on these ones block the Module A takes the decision of which inversion should be performed for the link power reduction. For this module is satisfied means the output is set to _1'. None of the output is set to _1' if there is no inversion is takes place. The module A is implemented using full adder and comparator circuit.

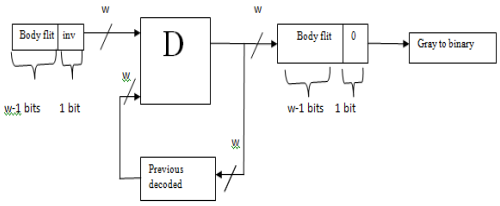

Fig.3. Block diagram for Decoder

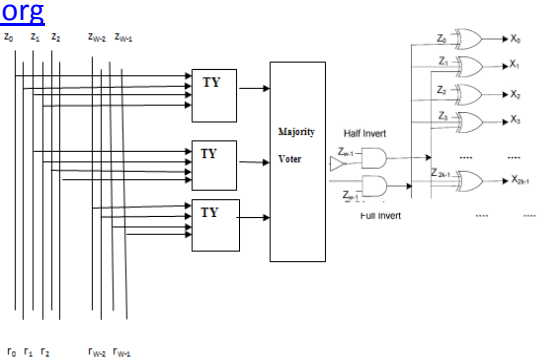

Fig.4. Internal view of Decoder block Scheme II

The block diagram of the decoder is shown in Fig.3. The w-1 bits input is applied in the decoder circuit and another input of the decoder is previous decoded output. The decoder block compares the two input data's and inversion operation is performed and w-1 bits output is produced. The remaining one bit is used to indicate the inversion is performed or not. Then the decoder output is given to the gray to binary block. This block converts the gray code into original binary input. In decoder circuit diagram (Fig.4.) consist of TY block and Majority vector and Xor circuits. Based on the encoder action the TY block is determined the transitions. Based on the transitions types the majority blocks checks the validity of the inequality given by(2). The output of the majority voter is given to the Xor circuit. Half inversion, full inversion and no inversion is performed based on the logic gates.

C. *Scheme III:*

In scheme III, we are adding the even inversion into scheme II. Because the odd inversion converts Type I transitions into Type II transitions. From table II, T_{1} **/T_{1}*** are converted into Type IV/Type III transitions by the flits is even inverted. The link power reduction in even inversion is larger than the Odd inversion.

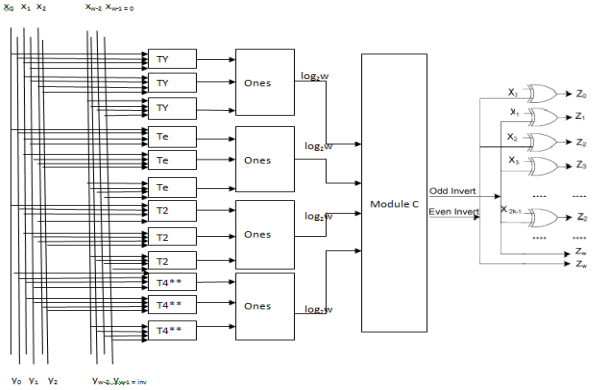

Fig.5 Encoder block Diagram Scheme III

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The encoding architecture (Fig.5) in scheme III is same of encoder architecture in scheme I and II . Here we adding the Te block to the scheme II. This is based on even invert condition, Full invert condition and Odd invert condition. It consist of w-1 link width input and the w bit is used for the inversion bit. The full, half and even Inversion is performed means the inversion bit is set _1', otherwise it set as _0'.The TY, Te and T4** block determines the transition types T2, Te and T4**. The transition types are send to the number of ones block. The Te block is determined if any of the detected transition of types T_2, T_1** and T_1**. The ones block determines the number of ones in the corresponding transmissions of TY, T2, Te and T4**. These number of ones is given to the Module C block. This block check if odd, even, full or no invert action corresponding to the outputs _10', _01', _11' or _00' respectively, should be performed. The decoder architecture of scheme II and scheme III are same.

IV RESULT AND DISCUSSION

Fig.6. shows the simulation result of scheme III (Type I (T_1***) using encoding techniques. In scheme II the number of type II transition is converted into Type IV transitions by using the odd and full inversion condition.Fig.7. shows the simulation result of Scheme III (Type I(T_1***) Decoder block output.

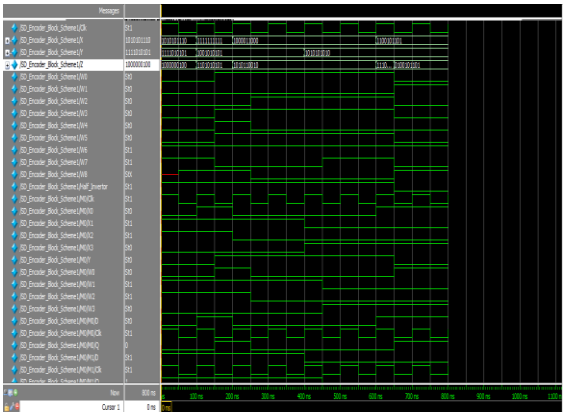

Fig.6. Simulation Result for Encoder Block Scheme III

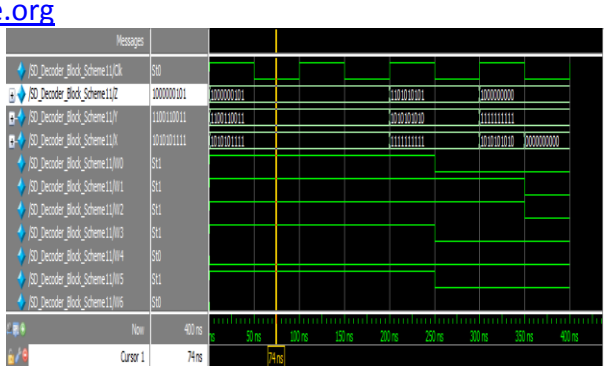

Fig.7. Simulation Result for Decoder block Scheme III

Fig.8 shows area calculation of encoding and decoding block.Area is reduced to less than 5% compared to data encoding [1].

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	21	7,168	1%	
Logic Distribution				
Number of occupied Slices	12	3,584	1%	
Number of Slices containing only related logic	12	12	100%	
Number of Slices containing unrelated logic	0	12	0%	
Total Number of 4 input LUTs	21	7,168	1%	
Number of bonded IOBs	28	141	19%	
Total equivalent gate count for design	129			
Additional JTAG gate count for IOBs	1,344			

Fig.8 Area analysis for Encoding Method

V CONCULSION

In this work, the encoding technique is implemented for reducing the transition activity in the NOC. This encoding scheme aimed at reducing the power dissipated by the links of an NOC. The proposed encoding schemes are agnostic with respect to the underlying NOC architecture in the sense that our application does not require any modification neither in the links nor in the links. The proposed architecture is coded using VERILOG language and is simulated and synthesized using Modelsim and Xilinx software. Overall, the application scheme allows 40% power saving and with less than 5% area overhead in the NI compared to the data encoding scheme.

In the future, the Network On Chip (NOC) implementation using different types of router and network interface technique will be analyzed . Comparing the area, delay and power with previous techniques.

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