IJETIE International Journal of Emerging Technology and Innovative Engineering
Volume I, Issue 3, March 2015
ISSN: 2394 - 6598
www.ijetie.org

An Efficient Design of Modified Booth Recoder for Fused Add-Multiply operator

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***Abstract*— For computing complex arithmetic calculations in DSP, the fused Add-Multiply (FAM) operator is optimized to increasing the performance. The Sum to Modified Booth algorithm is introduced for Add-Multiply operation. We look into, the technique to implement the direct recoding of sum of two numbers in its Modified Booth (MB) form. It is structured, simple and can be easily modified in order to be applied either in signed or unsigned numbers, which comprise of odd or even number of bits. It decreases the critical path delay and reduces area and power consumption.**

***Index Terms*— Add-Multiply operation, arithmetic circuits, Modified Booth recoding, VLSI design.**

I. Introduction

Now-a-days Electronics are mostly used for Digital Signal Processing(DSP).DSP application carryout large number of operation such as Discrete Cosine Transform and Fast Fourier Transform etc..,

The design of arithmetic components combining operation which shares data, can lead to significant performance improvements. Based on the observation addition can often be used to a multiplication.MAC will be used for this operation. The fast multiplication process consists of three Steps: partial product generation, partial product reduction and final carry-propagating addition. To reduce the number of partial products, recoding techniques have been widely used.
In addition, the multiply-accumulate (MAC) operation is very prevalent in many scientific and engineering applications. It is very easy to find such operation in signal processing algorithms and matrix arithmetic.

In this paper, we have to use S-MB recoding algorithm to reduce the partial product. S-MB operates direct recoding of sum of two numbers in its MB form leads to more efficient implementation of the Fused Add-multiply (FAM) unit compared to existing one, Conventional recoding schemes are based on the complex manipulation in bit-level, which are implemented by the gate level circuits. This work observe on the efficient design of the FAM operator, The aim of computing the of the recoding scheme for direct shaping of the MB form of sum of two numbers(Sum to Modified).We introduce the technique, which decrease the critical path delay and reduces area and power consumption. The proposed S-MB algorithm structured is simple and easily modified in order to apply either in signed or unsigned numbers which comprise odd or even number of bits. We explore three alternative schemes of the proposed S-MB approach using conventional and signed-bit Full Adders (FAs) and Half Adders (HAs) as building blocks. We evaluated the performance of the proposed S-MB technique by comparing its three different schemes with the state-of the-art recoding techniques. The proposed designs deliver improvements in both area occupation and power consumption, thus outperforming the existing S-MB recoding solutions. The rest of the paper is organized as follows: In section II, we discuss the motivation and present a technical background for the implementation of FAM units. In section III the proposed S-MB recoding schemes is presented .In Section IV, both theoretical analysis and experimental evaluation are given, clearly identifying the advantages of the proposed schemes with respect to area complexity, critical delay and power dissipation. Section V concludes our work.

II. Motivation and Implementation

In this paper, we observe on AM units which implement the operation Z=X.(A+B)The Existing design of the AM operator requires that its input B and C are driven to an adder and then the input A and the sum Y=A+B are driven to a multiplier in order to get X. The recent research activities in the field of arithmetic optimization have shown that the design of arithmetic components combining operations which share data, can lead to significant performance improvements. Based on the observation that an addition can often be subsequent to a multiplication (e.g., in symmetric FIR filters), the Multiply-Accumulator (MAC) and Multiply-Add (MAD) units were introduced leading to more efficient implementations of DSP algorithms compared to the conventional ones, which use only primitive resources. Several architectures have been proposed to optimize the performance of the MAC operation in terms of area occupation, critical path delay or power consumption. MAC components increase the flexibility of DSP data path synthesis as a large set of arithmetic operations can be efficiently mapped onto them. Except the MAC/MAD operations, many DSP applications are based on Add-Multiply (AM) operations. The straightforward design of the AM unit, by first allocating an adder and then driving its output to the input of a multiplier, increases significantly both area and critical path delay of the circuit.

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The proposed S-MB algorithm is structured, simple and can be easily modified in order to be applied either in signed (in 2's complement representation) or unsigned numbers, which comprise of odd or even number of bits. It explores three alternative schemes of the proposed S-MB approach using conventional and signed-bit Full Adders (FAs) and Half Adders (HAs) as building blocks. The proposed method evaluates the performance of the proposed S-MB technique by comparing its three different schemes with the state-of the- art recoding techniques. Industrial tools for RTL synthesis and power estimation have been used to provide accurate measurements of area utilization, critical path delay and power dissipation regarding various bit-widths of the input numbers. We show that the adoption of the proposed recoding technique delivers optimized solutions for the FAM design enabling the targeted operator to be timing functional (no timing violations) for a larger range of frequencies. Also, under the same timing constraints, the proposed designs deliver improvements in both area occupation and power consumption, thus outperforming the existing S-MB recoding solutions.

A.REVIEW OF THE MODIFIED BOOTH FORM

Modified Booth (MB) is a prevalent form used in multiplication. It is a redundant signed-digit radix-4 encoding technique. Its main advantage is that it reduces by half the number of partial products in multiplication comparing to any other radix-2 representation. Let us consider the multiplication of 2's complement numbers and with each number consisting of n=2kbits. The multiplicand can be represented in MB form as:

$y_j^{MB} \in \{-2, -1, 0, +1, +2\}, 0 \le j$ correspond to the three consecutive bits and with one bit overlapped and considering that Table I shows how they are formed by summarizing the MB encoding technique. Each digit is represented by three bits named , one and two. Using these three bits we calculate the MB digits by the following relation:

$$y_j^{MB} = (-1)^{s_j}.[(one_j+2.two_j)]$$

Binary			y_j^{MB}	MB encoding			Input Carry
y_{2j+1}	y_{2j}	y_{2j-1}		Sign=	1=	2=	$c_{in,j}$
0	0	0	0	0	0	0	0
0	0	1	+1	0	1	0	0
0	1	0	+1	0	1	0	0
0	1	1	+2	0	0	1	0
1	0	0	-2	1	0	1	1
1	0	1	-1	1	1	0	1
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	1	0
0	0	0	0	0	0	0	0

Table I. Modified Booth Encoding Table

B. FAM IMPLEMENTATION

The FAM design is presented in Figure I the multiplier is a parallel one based on the MB algorithm. Let us consider the product X.Y. The term is encoded based on the MB algorithm and multiplied. Both X and Y consists of n=2kbits and are in 2´s complement form.

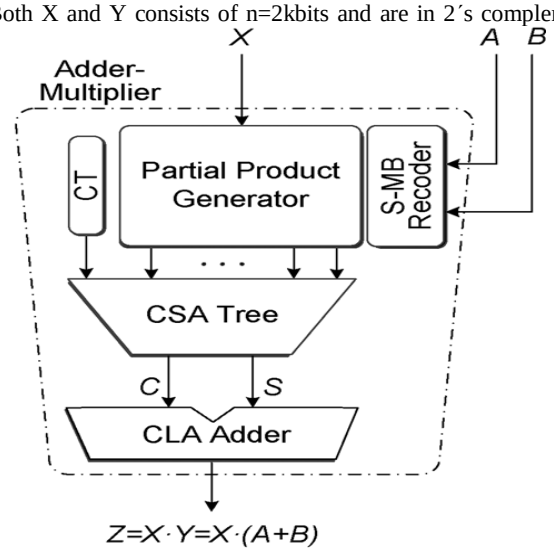

Fig I: Fused Add-Multiply

III.SUM TO MODIFIED BOOTH RECODING TECHNIQUE (S-MB)

A.Defining Signed-Bit Full Adders and Half Adders for Structured Signed Arithmetic

In S-MB recoding technique, it recodes the sum of two consecutive bits of the input A (a_{2j}, a_2) with two consecutive bits of the input B (b_{2j}, b_2) into one MB digit. The most significant of them is negatively weighted while the two least significant of them have positive weight. Consequently, in order to transform the two aforementioned pairs of bits in MB form we need to use signed-bit arithmetic. For this purpose, we develop a set of bit-level signed Half Adders (HA) and Full Adders (FA) considering their inputs and outputs to be signed.

1) S-MB1 Recoding Scheme:

The first scheme of the proposed recoding technique is referred as S-MB1
For both even and odd bit-width of input numbers

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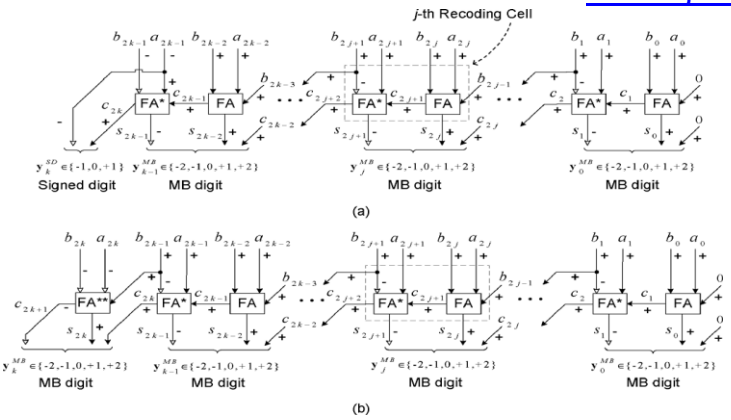

Fig .S-MB1 recoding scheme for a) Even and b) Odd number of bits

Both bits and are extracted from the j recoding cell. A conventional FA with inputs A and B produces the carry

2) S-MB2 Recoding Scheme:

The second approach of the proposed recoding technique, S-MB2, is described for even and odd bit-width of input numbers.

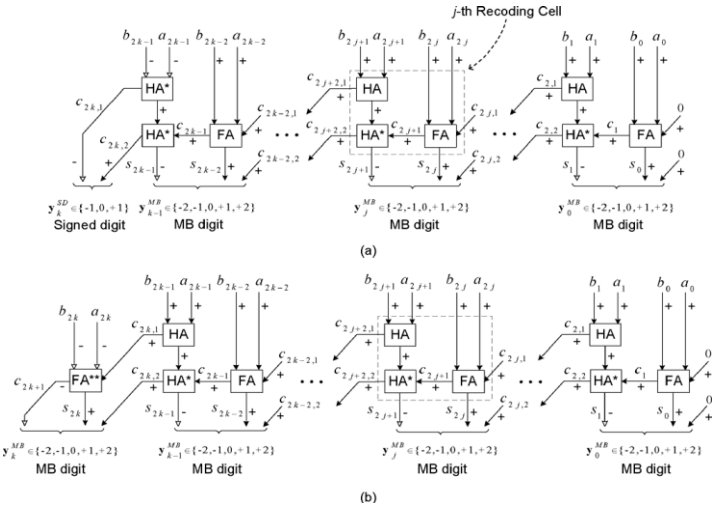

Fig .S-MB2 recoding scheme for a) Even and b) Odd number of bits

The third scheme implementing the proposed recoding technique is S-MB3. It consider that $C_{0,1}$=0 and $C_{0,2}$=0. It build the digits based on S_{2j+1},S_{2j} and $C_{2j,2}$, and according to (3.8). Once more, it use a conventional FA to produce the carry C_{2j+1} and the sum S_{2j}.

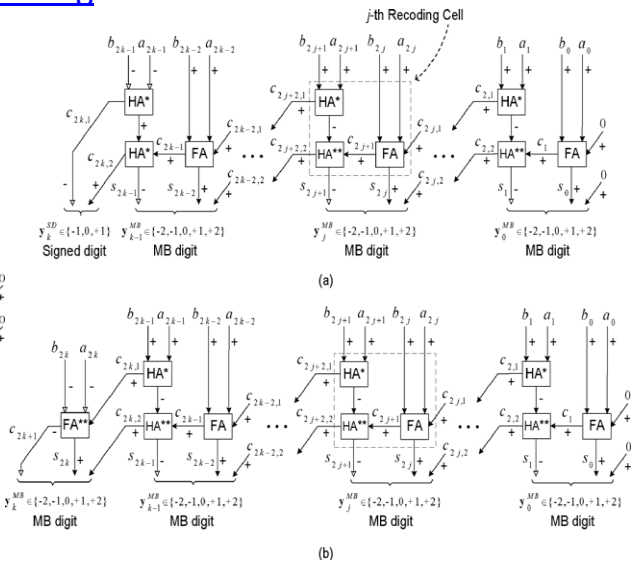

Fig .S-MB3 recoding scheme for a) Even and b) Odd number of bits

The bit is now the output carry of a HA* (basic operation Table 3.2), which belongs to the (j-1) recoding cell and has the bits , as inputs. The negatively signed bit is produced by a HA** (Table 3.4) in which we drive and the output sum (negatively signed) of the HA* of the j recoding cell with the bits as inputs. The carry and sum outputs of the HA** are given by the following Boolean equations:

$$= \quad c_{2j+}$$

$$s_{2j+1} = a_{2j+1} \oplus \qquad (3.15)$$

In case that both and comprise of even number of bits and are negatively weighted and this method use the dual implementation of the HA* (Table 3.3) in the (k-1) recoding cell. Consequently, the output sum of the HA* becomes positively weighted and the HA** that follows has to be replaced with a HA*. The most significant digits for both cases of even and odd bit-width of A and B are formed as in *S-MB*2 recoding scheme. The critical path delay of *S-MB*3 recoding scheme is calculated as follows:

$$T_{S-MB3} = T_{HA*,carry} + T_{FA,carry} + T_{HA**,sum}$$

IV.PERFORMANCE EVALUATION

A.Theoritical Analysis

In this section, we present a theoretical analysis and comparative study in terms of area complexity and critical delay among the three recoding schemes that we described in Section III and the three existing recoding techniques

TABLE-II Area And Delay Of Various Components In The Unit Gate Model.

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Components	Area (Gate equivalents)	Delay (Gate equivalents)
NAND-2, NOR-2	A_g	T_g
NAND-3, NOR-3	$2A_g$	$2T_g$
XOR, XNOR	$2A_g$	$2T_g$
HA	$3A_g$	$T_{HA,carry}=T_g$, $T_{HA,sum}=2T_g$
FA	$7A_g$	$T_{FA,carry}=3T_g$, $T_{FA,sum}=4T_g$

B.EXPERIMENTEL EVALUATION

In this section, we compare the performance of the three proposed recoding schemes explored in Section III with the three schemes described in [12], [13], [23].We included each of the recoding schemes in a fused Add-Multiply (FAM) operator (Fig. 1(b)) and implemented them using structural Verilog HDL for both cases of even and odd bit-width of the recoder's input numbers. The Wallace CSA tree and the fast CLA adder have been imported from the Synopsys DesignWare Library. We used Synopsys Design Compiler [18] and the Faraday 90 nm standard cell library [22] to synthesize the evaluated designs. In order to have a fair comparison among all FAM designs, they are implemented identically except for the recoding module.

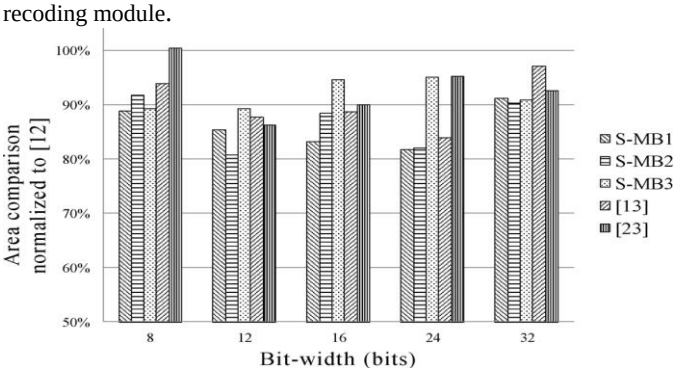

Fig. 4. Area comparison for even bit-width with all values normalized to the corresponding ones of [12].

CONCLUSION

This paper focuses on optimizing the design of the Fused-Add Multiply (FAM) operator. We propose a structured technique for the direct recoding of the sum of two numbers to its MB form. We explore three alternative designs of the proposed *S-MB* recoder and compare them to the existing. The proposed recoding schemes, when they are incorporated in FAM designs, yield considerable performance improvements in comparison with the most efficient recoding schemes found in literature.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for their constructive comments.

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